// Invocation args: -check -upper -ground\_nodes:GROUND -xprobe /home/Mentor\_Graphics/pyxis/Pyxis\_v17.2\_p201706036\_rhel6or7/tmp/home/work/jathin/vlsi/rca\_tb/RCA/eldo.nspice\_xprobe -eldo -o $JATHIN/vlsi/rca\_tb/RCA/netlist.spi -log /home/work/jathin/vlsi/rca\_tb/RCA/netlist\_transcript -quiet $JATHIN/vlsi/rca\_tb/RCA

// \*\*\*\* Reading <$JATHIN/vlsi/rca\_tb/RCA> for ELDO netlist \*\*\*\*

// Checking 3 sheet(s) for out of date references to symbols and interfaces...

// Done.

// Parsing file '/home/Mentor\_Graphics/pyxis/Pyxis\_v17.2\_p201706036\_rhel6or7/mgc\_icstd\_lib//global.ncf' succeeded.

// NOTE: There is no part interface for the top level schematic. The external nets in the schematic

// are being scanned to create the pin names for the top level subckt.

Processing [$JATHIN/vlsi/rca\_tb] [rca\_tb/rca\_tb] [schematic] (NCF entry line: 17 file: $NCF\_GLOBAL)

Processing [$JATHIN/vlsi/rca] [rca/rca] [rca] (NCF entry line: 17 file: $NCF\_GLOBAL)

Processing [$JATHIN/vlsi/full\_adder] [full\_adder/full\_adder] [full\_adder1] (NCF entry line: 17 file: $NCF\_GLOBAL)

Primitive [/home/Mentor\_Graphics/pyxis/Pyxis\_v17.2\_p201706036\_rhel6or7/mgc\_icstd\_lib/mgc\_ic\_macrolib/or] [or/or] [ELDOSPICE=OR2\_] (NCF entry line: 1638 file: $NCF\_GLOBAL)

Primitive [/home/Mentor\_Graphics/pyxis/Pyxis\_v17.2\_p201706036\_rhel6or7/mgc\_icstd\_lib/mgc\_ic\_macrolib/and] [and/and] [ELDOSPICE=AND2\_] (NCF entry line: 1503 file: $NCF\_GLOBAL)

Primitive [/home/Mentor\_Graphics/pyxis/Pyxis\_v17.2\_p201706036\_rhel6or7/mgc\_icstd\_lib/mgc\_ic\_macrolib/xor] [xor/xor] [ELDOSPICE=XOR] (NCF entry line: 1563 file: $NCF\_GLOBAL)

Primitive [$MGC\_IC\_SOURCES\_LIB/pattern\_v\_source] [pattern\_v\_source/pattern\_v\_source] [SPICE=V] (NCF entry line: 675 file: $NCF\_GLOBAL)

Primitive [$MGC\_IC\_SOURCES\_LIB/dc\_v\_source] [dc\_v\_source/dc\_v\_source] [SPICE=V] (NCF entry line: 565 file: $NCF\_GLOBAL)

\*\*\*\* Writing <$JATHIN/vlsi/rca\_tb/RCA> netlist for ELDO \*\*\*\*

**Number of cells: 8**

**Number of primitive instances: 30**

Done...

Running eldo on localhost.localdomain

with Eldo libraries :

/home/Mentor\_Graphics/ams/aol/lib/libeldoudm\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldomos1\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldoekv\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldomosp9\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldocsem\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldomos2\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldomos3\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldobip\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldodio\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldojfet\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldosoi\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldomos4\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldoasitft\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldohisim\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldospmod\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldopsp\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldomosvar\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldolegtft\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldosimkit\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldomoto\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldost\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldobnr\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldorockw\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldopubhicum\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldotftsh\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldobta\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldofas\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldofascm\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldosdsim\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libeldowire\_64.so

/home/Mentor\_Graphics/ams/aol/lib/libogr\_64.so loaded.

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\*\*\*\*\* SYSTEM INFORMATION ...

\*\*\* User : root

\*\*\* OS : CentOS release 6.5 (Final) [VCO = aol]

\*\*\* CPU :

12th Gen Intel(R) Core(TM) i3-12100

**Number of physical processors : 8**

Hyper-Threading Technology : N/A

Number of cpu cores : N/A

Number of logical processors : N/A

\*\*\* Freq : 3302.404MHz

\*\*\* Cache : 12288 KB

\*\*\* MEM : 8045632 kB

\*\*\* Date : Thu Feb 1 21:39:39 2024

\*\*\* Eldo VERSION : ELDO 17.1 patch1 (64 bits) Thu Apr 6 15:28:32 GMT 2017

\*\*\*\*\* PRE-PROCESSING ...

\*\*\*\*\* ANALYSIS ....

Warning 206: In file "./netlist.spi" line 15:

+ OBJECT "OR2\_\_OR1": Parameter or model not defined yet. Make sure that it was not an instance which was meant rather than an Eldo LOGIC primitive.

Warning 206: In file "./netlist.spi" line 16:

+ OBJECT "AND2\_\_AND2": Parameter or model not defined yet. Make sure that it was not an instance which was meant rather than an Eldo LOGIC primitive.

Warning 206: In file "./netlist.spi" line 17:

+ OBJECT "AND2\_\_AND1": Parameter or model not defined yet. Make sure that it was not an instance which was meant rather than an Eldo LOGIC primitive.

Warning 206: In file "./netlist.spi" line 18:

+ OBJECT "XOR1": Parameter or model not defined yet. Make sure that it was not a subcircuit which was meant rather than an Eldo LOGIC primitive.

Warning 206: In file "./netlist.spi" line 19:

+ OBJECT "XOR2": Parameter or model not defined yet. Make sure that it was not a subcircuit which was meant rather than an Eldo LOGIC primitive.

Warning 46: In file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 6767:

+ Double definition for parameter ISA

+ Previous definition was in file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 8

Warning 46: In file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 6767:

+ Double definition for parameter BFA

+ Previous definition was in file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 8

Warning 46: In file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 6767:

+ Double definition for parameter NFA

+ Previous definition was in file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 8

Warning 46: In file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 6767:

+ Double definition for parameter RBA

+ Previous definition was in file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 8

Warning 46: In file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 6767:

+ Double definition for parameter REA

+ Previous definition was in file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 8

Warning 46: In file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 6767:

+ Double definition for parameter RCA

+ Previous definition was in file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 8

Warning 46: In file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 6767:

+ Double definition for parameter RBMA

+ Previous definition was in file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 8

Warning 46: In file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 6767:

+ Double definition for parameter CJEA

+ Previous definition was in file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 8

Warning 46: In file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 6767:

+ Double definition for parameter CJCA

+ Previous definition was in file "/home/Mentor\_Graphics/FOUNDRY/GDK/Pyxis\_SPT\_HEP/ic\_reflibs/tech\_libs/generic13/models/lib.eldo" line 8

\*\*\*\*\* 0 error(s).

\*\*\*\*\* 14 warning(s).

\*\*\*\*\* GENERATION ...

Warning 1615: In file "./rca\_tb\_RCA\_default.cir" line 11:

+ COMMAND ".TRAN": TPRINT can not be <= 0.0.

+ It is set to TSTOP/20.0 = 5.000e-08 s.

Warning 107: NODE "VDD": Less than two connections.

\*\*\*\*\* 0 error(s).

\*\*\*\*\* 16 warning(s).

INFORMATION ABOUT COMPILATION...

Peak memory usage (MB): 41

Virtual memory usage (MB): 371

**30 elements**

**30 nodes**

**30 input signals**

\*\*\*> Parsing CPU TIME 0h 0mn 0s 070ms <\*\*\*

\*\*\* DATE: 1-Feb-2024 21:39:39

\*\*\* TITLE: \* Component: $JATHIN/vlsi/rca\_tb Viewpoint: RCA

TEMPERATURE : 27.000000 degrees C

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Summary of situations encountered in the circuit

which can cause simulation issues:

Missing connections: 1 occurrence(s)

Name of one of such node involved: VDD

Work-around applied: No

You may consider .OPTION RGND = #

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Performing DC analysis...

--> Partitioning circuit...

\*\*\*> DC CPU TIME 0s 010ms <\*\*\*

DC:1 iterations FOR DC analysis

C0 0.0000

CAR 0.0000

M1 0.0000

M2 0.0000

M3 0.0000

M4 0.0000

N1 0.0000

N2 0.0000

N3 0.0000

N4 0.0000

O1 0.0000

O2 0.0000

O3 0.0000

O4 0.0000

VDD 5.0000

X\_RCA1.N$20 0.0000

X\_RCA1.N$25 0.0000

X\_RCA1.N$30 0.0000

X\_RCA1.X\_FULL\_ADDER1.N$18 0.0000

X\_RCA1.X\_FULL\_ADDER1.N$22 0.0000

X\_RCA1.X\_FULL\_ADDER1.N$24 0.0000

X\_RCA1.X\_FULL\_ADDER2.N$18 0.0000

X\_RCA1.X\_FULL\_ADDER2.N$22 0.0000

X\_RCA1.X\_FULL\_ADDER2.N$24 0.0000

X\_RCA1.X\_FULL\_ADDER3.N$18 0.0000

X\_RCA1.X\_FULL\_ADDER3.N$22 0.0000

X\_RCA1.X\_FULL\_ADDER3.N$24 0.0000

X\_RCA1.X\_FULL\_ADDER4.N$18 0.0000

X\_RCA1.X\_FULL\_ADDER4.N$22 0.0000

X\_RCA1.X\_FULL\_ADDER4.N$24 0.0000

**TOTAL POWER DISSIPATION: 0.0000 WATTS**

Eldo NEWTON: VNTOL=1.000000e-06 RELTOL=1.000000e-03

Connecting to JWDB server, please wait...

connected to wdb server : -jwdbhost localhost.localdomain -jwdbport 37761

Compute from 0.000000 Nano to 1.000000E+03 Nano

................................................

Simulation progress : 10% (t = 149.5000 N)

Elapsed CPU time : 0h 0mn 0s 10 ( 0h 0mn 0s 10)

CPU Usage : 100% (100%)

................................................

Simulation progress : 20% (t = 200.1261 N)

Elapsed CPU time : 0h 0mn 0s 0 ( 0h 0mn 0s 10)

CPU Usage : 0% (100%)

................................................

Simulation progress : 30% (t = 300.1261 N)

Elapsed CPU time : 0h 0mn 0s 0 ( 0h 0mn 0s 10)

CPU Usage : 100% (100%)

................................................

Simulation progress : 40% (t = 403.2577 N)

Elapsed CPU time : 0h 0mn 0s 0 ( 0h 0mn 0s 10)

CPU Usage : 0% (100%)

................................................

Simulation progress : 50% (t = 580.3107 N)

Elapsed CPU time : 0h 0mn 0s 0 ( 0h 0mn 0s 10)

CPU Usage : 100% (100%)

................................................

Simulation progress : 70% (t = 763.0750 N)

Elapsed CPU time : 0h 0mn 0s 0 ( 0h 0mn 0s 10)

CPU Usage : 100% (100%)

................................................

Simulation progress : 100% (t = 1.0000 U)

Elapsed CPU time : 0h 0mn 0s 0 ( 0h 0mn 0s 10)

CPU Usage : 100% (100%)

\*\*\*>Current simulation completed

SIMULATION INFORMATION

Peak memory usage (MB): 45

Virtual memory usage (MB): 371

Latency: 0.000000%

average number of newton iterations: 1.000000

nb of components: 30

nb of nodes: 30

nb of MOS or BIP calls: 0

Number of steps computed: 201

\*\*\*>CPU TIME 0s 010ms <\*\*\*

\*\*\*>MESSAGE SUMMARY: 16 warnings

\*\*\*>GLOBAL CPU TIME 0s 150ms <\*\*\*

\*\*\*>GLOBAL ELAPSED TIME 1s <\*\*\*

-----------------------------------------

Maximum number of license(s) consumed:

1 Analog Simulator Kernel (eldokernel)

Time spent acquiring licenses: 0.036631 s (avg: 0.036631 s, max: 0.036631 s at Thu Feb 1 21:39:39 2024)

Time spent releasing licenses: 0.000849 s (avg: 0.000849 s, max: 0.000849 s at Thu Feb 1 21:39:40 2024)

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